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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,400	04/12/2004	German R. Gutierrez	BU1647C2	2892

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,400	GUTIERREZ ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *1-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 25, 2008 has been entered.

Claim Objections

2. Claims 1-8 are objected to because of the following informalities:

According to the embodiment of the present invention shown in Figure 10, the following changes are suggested by the examiner.

Claim 1, line 3, “a reference signal” should be “an oscillator signal”.

Claim 1, line 5, “the reference signal” should be “the oscillator signal”.

Claim 1, lines 15-16, “an oscillator signal” should be “the oscillator signal as the output signal”.

Claims 2-8 depend either directly or indirectly from the independent claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 3 further recites the steps of receiving at a frequency divider coupled to the oscillator the oscillator signal and dividing the oscillator signal for generating the reference signal. Clearly, as shown in Figure 10 and discussed in the specification of the present invention, the divider (1024) divides the oscillator signal from the oscillator (1022) and generates a reference signal to the phase/frequency detector (1030) of the other circuit, not the phase detector (1010) as recited in the precedent claim 1. Therefore, claim 3 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volk (U.S. Patent No. 5,384,502) in view of Everitt et al. (U.S. Patent No. 6,188,739, hereinafter "Everitt") and Takashi et al. (U.S. Patent No. 5,805,024, hereinafter "Takashi").

Regarding claim 1, Volk discloses a phase locked loop (PLL) circuit 60 in Figure 3 comprising a phase comparison circuit 61 which receives an external data input signal Θ_D and a reference signal Θ_{FB} to generate a phase detected output signal (PD and/or UP) indicative of a difference between the input signal and the reference signal; a split loop filter 63 which filters the phase detected output signal through a charge pump 62 to provide a filtered output signal; a trans-conductance (gm) amplifier 64 which amplifies the filtered output signal to generate a current output signal I_{OS}; a variable gain current source 65 which receives the current output signal I_{OS} and a first current output signal I_{OS1} to generate a second current output signal I_{OS2}; a VCO 66 which receives the

second current output signal I_{OS2} to generate an oscillator signal; and a frequency divider 67 which divides the frequency of the oscillator signal to generate the reference signal.

Volk fails to show, teach or suggest that a second filter is used coupled between the trans-conductance (gm) amplifier 64 and the VCO 66 to further filter the current output signal I_{OS} from the trans-conductance (gm) amplifier 64 before controlling the oscillator signal of the VCO 66.

Everitt also discloses a PLL circuit 400 in Figure 4 comprising similar circuitries of Volk's PLL circuit. Further, the PLL circuit also includes a second integrator (second filter) 450 coupled between a charge pump (sometime also called trans-conductance (gm) amplifier) and a signal controlled oscillator (VCO) 416 to generate a current signal to the VCO 416 in order to generate a reference signal to the phase or frequency comparator circuit 404. Also see Col. 4, line 39 to Col. 5, line 18.

Volk also fails to show, teach or suggest that a multiplexer is coupled to the gm amplifier 64 in the feed forward path of the PLL circuit 60 and another device to select one of the current output signals of the gm amplifier and the other circuit to VCO 66 through the variable gain current source 65.

Takashi also discloses a PLL circuit 128 in Figure 4 comprising similar circuitries of Volk's PLL circuit, for example, a first phase comparator 231, a second phase comparator 131, a numerical value converter 232, a switch 233, a current converting circuit 140, a filter circuit 133, and a VCO 136, which generates a sampling clock to the first phase comparator 231. The switch 233 selects either a first phase output from the

first phase comparator 231 or a second phase output from the second phase comparator 131 to generate a current signal to the filter circuit 133 through the current correcting circuit 140 based on a reference control signal controlled by a sequencer 129. Col. 7, lines 4-16.

Therefore, it would have been obvious to one of ordinary skill in the art to add an additional filter prior Volk's VCO 66 of the PLL circuit 60 as taught by Everitt for the purpose of further or additionally filtering, for example, the current signal of the trans-conductance (gm) amplifier 64 prior controlling the frequency by the VCO 66. It is also obvious to one of ordinary skill in the art to provide a multiplexer or switch circuit in the feed forward path of Volk's PLL circuit as taught by Takashi in order to select one of a current signal, for example, from either the first phase comparator 231 or the second phase comparator 131 to the VCO 66 to generate a voltage control oscillator signal, for instance, for the purpose of reducing the phase locked time in Volk's PLL circuit.

Regarding claim 2, the split loop filter 63 shown in Figure 4 is indicated as a single-pole RC filter.

Regarding claim 3, the frequency divider 67 is coupled to the VCO 66 and divided the oscillator signal to generate the reference signal to the phase comparison circuit 61.

Regarding claim 4, the external data input signal Θ_D is a serial data stream.

Regarding claim 5, it is well known to an artisan to know that the serial data stream of the external data input signal Θ_D could be operated at a data rate of at least 2.488 Ghz if Volk's PLL circuit 60 is used in a SONET OC-48 transceiver as pointed out

at least in the Background of the Invention of the instant application on page 3, lines 8-12.

Regarding claim 8, the reference signal used in the phase comparison circuit 61 is a reference clock signal generated by the VCO 66 through the frequency divider 67.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk in view of Everitt and Takashi as applied to claim 1 above, and further in view of Voorman (U.S. Patent No. 4,780,690).

Regarding claim 6, although Volk discloses that the trans-conductance (gm) amplifier 64 shown in Figure 4 comprises amplifiers receiving the filtered signal of the split loop filter 63 and a current load circuit coupled to the amplifiers to provide the current signal $I_{OS,}$ Volk fails to teach or suggest that the amplifiers are differential amplifiers.

Voorman relates to a filter arrangement having a trans-conductance circuit shown in Figure 1, wherein the trans-conductance circuit, for example, shown in Figure 3 comprises two differential amplifiers receiving the filtered signal of the filter arrangement of Figure 1 and a current load circuit I_5 coupled to the differential amplifiers to provide a current signal. Also see Col. 5, lines 1-24.

Therefore, it would have been obvious to one of ordinary skill in the art that Volk's trans-conductance (gm) amplifier 64 of the PLL circuit 60 is capable of or being integrated by a differential amplifier and a current load circuit as taught by Voorman in order to generate a current signal from a current of a filter.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk in view of Everitt and Takashi as applied to claim 1 above, and further in view of Hotine (U.S. Patent No. 4,656,647).

Regarding claim 7, although Volk does not show, teach or suggest that the output signal of the phase comparison circuit 61 of the PLL circuit 60 has a peak to peak signal swing of less than one volt.

Hotine discloses a PLL circuit in Figure 2 comprising a phase comparator 45, a low pass filter 48 and a VCO 50, wherein the phase comparator 45 compares a voltage output signal 42 having a 0.2 peak to peak voltage through a squaring amplifier 43 with an oscillator voltage generated from the VCO 50. Obviously, the voltage at the output signal 47 of the phase comparator 45 has a peak to peak signal of less than one volt. Also see Col. 8, line 45 to Col. 9, line 25.

Therefore, it would have been obvious to one of ordinary skill in the art as taught by Hotine that Volk's phase comparison circuit 61 of the PLL circuit 60 is capable of generating a voltage swing, for example, has a peak to peak signal of less than one volt in order to reduce the voltage of a voltage supply of the PLL circuit 60.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is 571- 272-3051. The examiner can normally be reached on Monday-Friday 10:00-6:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on 571- 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/YOUNG T. TSE/
Primary Examiner, Art Unit 2611